CLAIMS

1. Apparatus for enabling an instruction to control data flow bypassing hardware within a processor of a programmable processing engine, the apparatus comprising:

a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback and execution stages, the execution stage having a plurality of parallel execution units; and

an instruction set of the processor, the instruction set defining a register decode value that specifies one of source operand bypassing and result bypassing from a previous instruction executing in pipeline stages of the processor.

2. The apparatus of Claim 1 further comprising:

a register file containing a plurality of general-purpose registers for storing intermediate result data processed by the execution units; and

a memory for storing one of transient data unique to a specific process and pointers referencing data structures.

3. The apparatus of Claim 2 wherein the register decode value comprises one of a result bypass (RRB) operand and an inter-unit result bypass (RIRB) operand, each of which explicitly controls data flow within the pipeline of the processor.

4. The apparatus of Claim 3 wherein the execution units comprise a current execution unit and an alternate execution unit, and wherein the RRB operand denotes the current execution unit and the RIRB operand denotes the alternate execution unit.

5. The apparatus of Claim 3 wherein the RRB operand explicity infers feedback of the data delivered from a current one of the execution units to an input register of the current execution unit over a feedback path.

6. The apparatus of Claim 5 wherein the writeback stage comprises an interstage register and wherein the RRB operand enables bypassing write-back of the data processed by the execution units to one of the register file or the interstage register of the writeback stage.

7. The apparatus of Claim 2 wherein the register decode value comprises a source bypass (RISB) operand that allows source operand data to be shared among the parallel execution units of the pipelined processor.

8. The apparatus of Claim 7 wherein the execution units comprise a main execution unit and a secondary execution unit, and wherein the RISB operand allows the secondary execution unit to receive data stored at an effective memory address specified by a displacement operand in the previous instruction executed by the main execution unit.

9. A method for enabling an instruction to control data flow bypassing hardware within a pipelined processor of a programmable processing engine, the method comprising the steps of:

defining a register decode value that specifies one of source operand bypassing and result bypassing from a previous instruction executing in pipeline stages of the processor; and

identifying a pipeline stage register for use as a source operand in an instruction containing the register decode value.

10. The method of Claim 9 further comprising the step of explicitly controlling data flow within the pipeline stages of the processor through use of a register result bypass (RRB) operand.

11. The method of Claim 10 wherein the pipeline stages include instruction decode, writeback and execution stages, and wherein the execution stage comprises multiple parallel execution units including a current execution unit and an alternate execution unit.

12. The method of Claim 11 wherein the step of explicitly controlling comprises the steps of:

retrieving data from the current execution unit; and

returning the data to an input execution register specified by the RRB operand, thereby bypassing write-back of the data to either a register file or memory at the write-back stage.

13. The method of Claim 12 wherein the step of identifying further comprises the steps of:

explicitly specifying the pipeline stage register to be used as the source operand for the instruction; and

obviating need to keep track of a scoreboard addressing area.

14. The method of Claim 13 wherein the step of obviating comprises the step of eliminating the need for a scoreboard data structure in the pipelined processor.

15. The method of Claim 14 further comprising the step of sharing source operand data among the parallel execution units of the pipelined processor through the use of a source bypass (RISB) operand.

16. The method of Claim 15 wherein the step of sharing comprises the step of receiving data at the alternate execution unit, the data stored at a memory address specified by a displacement operand in a previous instruction executed by the current execution unit of the processor.

17. The method of Claim 16 wherein the step of sharing further comprises the step of realizing two memory references through the use of a single bus operation over a local bus.

18. The method of Claim 17 wherein the step of sharing further comprises the step of encoding the RISB operand with substantially fewer bits than those needed for a displacement address.

19. A computer readable medium containing executable program instructions for enabling an instruction to control data flow bypassing hardware within a pipelined processor of a programmable processing engine, the executable program instructions comprising program instructions for:

defining a register decode value that specifies one of source operand bypassing and result bypassing from a previous instruction executing in pipeline stages of the processor; and

identifying a pipeline stage register for use as a source operand in a current instruction containing the register decode value.

20. The computer readable medium of Claim 19 further comprising program instructions for explicitly controlling data flow within the pipeline stages of the processor through use of a register result bypass operand.

21. The computer readable medium of Claim 20 further comprising program instructions for sharing source operand data among parallel execution units of the pipelined processor through the use of a source bypass operand.